What is claimed is:

1. A display system comprising:

a display panel including a plurality of pixels, a plurality of data lines, and a plurality of scan lines;

a display driver which drives the data lines; and

a display controller which supplies display data to the display driver and also controls the display driver,

wherein the display controller:

includes first to (j + 2)th data output terminals (where j is a natural number) for outputting (j + 2) bits of display data out of display data that is output in a k-bit unit (where k is an integer such that $k \geq j + 2$);

outputs display data in a j-bit unit to the display driver through the first to j-th data output terminals;

outputs command data for controlling the display driver instead of the (j + 1)th bit of display data, through the (j + 1)th data output terminal to the display driver; and

outputs a command identification signal for identifying the command data instead of the (j + 2)th bit of display data, through the (j + 2)th data output terminal to the display driver,

and wherein the display driver includes:

first to j-th data input terminals for inputting display data in a j-bit unit;

a latch which fetches the command data that is specified according to the command identification signal;

a decoder which decodes the command data fetched into the latch; and

a control section which outputs a control signal corresponding to a decoding result by the decoder, the display driver driving the data lines based on the control signal and the display data that has been input through the first to j-th data input

terminals.

2. A display system comprising:

a display panel including a plurality of pixels, a plurality of data lines, and a plurality of scan lines;

a display driver which drives the data lines; and

a display controller which supplies multiplexed data including display data to the display driver and also controls the display driver,

wherein the display controller:

includes first to (j + 1)th data output terminals (where j is a natural number) for outputting (j + 1) bits of display data out of display data that is output in a k1-bit unit (where k1 is an integer such that $k1 \geq j + 1$);

outputs multiplexed data in which display data and command data has been time-division multiplexed within one horizontal scan period, in a j-bit unit to the display driver through the first to j-th data output terminals; and

outputs a command identification signal for identifying the command data instead of the (j + 1)th bit of display data, to the display driver through the (j + 1)th data output terminal, and

wherein the display driver includes:

first to j-th data input terminals for inputting display data in a j-bit unit;

a latch which fetches command data from the multiplexed data, specified according to the command identification signal;

a decoder which decodes the command data fetched into the latch; and

a control section which outputs a control signal corresponding to a decoding result by the decoder; the display driver driving the data lines based on the control signal and the display data included within the multiplexed data that has been input through the first to j-th data input terminals.

3. A display system comprising:

a display panel including a plurality of pixels, a plurality of data lines, and a plurality of scan lines;

a display driver which drives the data lines; and

a display controller which supplies display data to the display driver and also controls the display driver;

wherein the display controller:

includes first to (j + p)th data output terminals (where j is a natural number) for outputting (j + p) bits of display data out of display data that is output in a k2-bit unit (where k2 and p are positive integers such that $k2 \geq j + p$);

outputs display data in a j-bit unit to the display driver through the first to j-th data output terminals; and

outputs command data instead of the (j + 1)th to (j + p)th bits of the display data through the (j + 1)th to (j + p)th data output terminals to the display driver, and

wherein the display driver includes:

first to j-th data input terminals for inputting display data in a j-bit unit;

a latch which fetches the command data;

a decoder which decodes the command data fetched into the latch; and

a control section which outputs a control signal corresponding to a decoding result by the decoder, the display driver driving the data lines based on the control signal and the display data that has been input through the first to j-th data input terminals.

4. The display system as defined by claim 1,

wherein, when j bits of display data include grayscale data for an R color component, a G color component and a B color component, number of bit of grayscale

data for the G color component is larger than number of bit of grayscale data for the R color component, and is also larger than number of bit of grayscale data for the B color component.

5. The display system as defined by claim 2,

wherein, when j bits of display data include grayscale data for an R color component, a G color component and a B color component, number of bit of grayscale data for the G color component is larger than number of bit of grayscale data for the R color component, and is also larger than number of bit of grayscale data for the B color component.

6. The display system as defined by claim 3,

wherein, when j bits of display data include grayscale data for an R color component, a G color component and a B color component, number of bit of grayscale data for the G color component is larger than number of bit of grayscale data for the R color component, and is also larger than number of bit of grayscale data for the B color component.

7. A display controller which controls a display driver which drives a data line of a display panel, based on display data which is input in a j-bit unit (where j is a natural number); the display controller including:

first to (j + 2)th data output terminals;

a mode setting register for setting an operation mode of the display controller to a first or second mode;

a command data output section which outputs command data for controlling the display driver and a command identification signal for specifying the command data; and

a display data output section which outputs display data in a k-bit unit (where k is an integer such that $k \geq j + 2$) or a j-bit unit,

wherein the display data output section:

outputs (j + 2) bits of display data out of display data that is output in a k-bit unit, through the first to (j + 2)th data output terminals, in a first mode; and

outputs display data in a j-bit unit through the first to j-th data output terminals, and also outputs command data instead of the (j + 1)th bit of display data through the (j + 1)th data output terminal and the command identification signal instead of the (j + 2)th bit of display data through the (j + 2)th data output terminal, in a second mode.

8. A display controller which controls a display driver which drives a data line of a display panel, based on display data which is input in a j-bit unit (where j is a natural number); the display controller comprising:

first to (j + 1)th data output terminals;

a mode setting register for setting an operation mode of the display controller to a first or second mode;

a command data output section which outputs a command identification signal for specifying command data for controlling the display driver; and

a display data output section which outputs multiplexed data in which display data in a k1-bit unit (where k1 is an integer such that $k1 \geq j + 1$) or a j-bit unit and the command data are multiplexed, within one horizontal scan period,

wherein the display data output section:

outputs the multiplexed data including (j + 1) bits of display data out of display data that is output in a k1-bit unit, through the first to (j + 1)th data output terminals, in a first mode; and

outputs the multiplexed data including display data in a j-bit unit through the first to j-th data output terminals, and also outputs the command identification signal at

a time corresponding to command data included within the display data instead of the (j + 1)th bit of display data, through the (j + 1)th data output terminal, in a second mode.

9. A display controller which controls a display driver which drives a data line of a display panel, based on display data which is input in a j-bit unit (where j is a natural number); the display controller comprising:

first to (j + p)th (where p is a natural number) data output terminals;

a mode setting register for setting an operation mode of the display controller to a first or second mode;

a command data output section which outputs command data for controlling the display driver; and

a display data output section which outputs display data in a k2-bit unit (where k2 is a positive integer such that $k2 \geq j + p$) or a j-bit unit,

wherein the display data output section:

outputs (j + p) bits of display data out of display data that is output in a k2-bit unit, through the first to (j + 2)th data output terminals, in a first mode; and

outputs display data in a j-bit unit through the first to j-th data output terminals, and also outputs command data instead of the (j + 1)th to (j + p)th bits of display data through the (j + 1)th to (j + p)th data output terminals, in a second mode.

10. The display controller as defined by claim 7,

wherein, when j bits of display data include grayscale data for an R color component, a G color component and a B color component, number of bit of grayscale data for the G color component is larger than number of bit of grayscale data for the R color component, and is also larger than number of bit of grayscale data for the B color component.

11. The display controller as defined by claim 8,

wherein, when j bits of display data include grayscale data for an R color component, a G color component and a B color component, number of bit of grayscale data for the G color component is larger than number of bit of grayscale data for the R color component, and is also larger than number of bit of grayscale data for the B color component.

12. The display controller as defined by claim 9,

wherein, when j bits of display data include grayscale data for an R color component, a G color component and a B color component, number of bit of grayscale data for the G color component is larger than number of bit of grayscale data for the R color component, and is also larger than number of bit of grayscale data for the B color component.

13. The display controller as defined by claim 7,

wherein, when display data includes grayscale data for an R color component, a G color component, and a B color component:

display data in which number of bit of grayscale data for each of the R color component, the G color component, and the B color component is the same is output in the first mode; and

display data in which number of bit of grayscale data for at least one of the R color component, the G color component, and the B color component is different is output in the second mode.

14. The display controller as defined by claim 8,

wherein, when display data includes grayscale data for an R color component, a G color component, and a B color component:

display data in which number of bit of grayscale data for each of the R color component, the G color component, and the B color component is the same is output in the first mode; and

display data in which number of bit of grayscale data for at least one of the R color component, the G color component, and the B color component is different is output in the second mode.

15. The display controller as defined by claim 9,

wherein, when display data includes grayscale data for an R color component, a G color component, and a B color component:

display data in which number of bit of grayscale data for each of the R color component, the G color component, and the B color component is the same is output in the first mode; and

display data in which number of bit of grayscale data for at least one of the R color component, the G color component, and the B color component is different is output in the second mode.

16. The display controller as defined by claim 10,

wherein, when display data includes grayscale data for an R color component, a G color component, and a B color component:

display data in which number of bit of grayscale data for each of the R color component, the G color component, and the B color component is the same is output in the first mode; and

display data in which number of bit of grayscale data for at least one of the R color component, the G color component, and the B color component is different is output in the second mode.

17. The display controller as defined by claim 11,

wherein, when display data includes grayscale data for an R color component, a G color component, and a B color component:

display data in which number of bit of grayscale data for each of the R color component, the G color component, and the B color component is the same is output in the first mode; and

display data in which number of bit of grayscale data for at least one of the R color component, the G color component, and the B color component is different is output in the second mode.

18. The display controller as defined by claim 12,

wherein, when display data includes grayscale data for an R color component, a G color component, and a B color component:

display data in which number of bit of grayscale data for each of the R color component, the G color component, and the B color component is the same is output in the first mode; and

display data in which number of bit of grayscale data for at least one of the R color component, the G color component, and the B color component is different is output in the second mode.